

REMARKS

Claims 1-40 are pending in this application, of which claims 22-24 have been amended.

Claims 1-21 and 25-32 are withdrawn from consideration. Claims 33-40 are newly-added.

The Examiner has indicated that FIGS. 29(A)-38 should be labeled "Prior Art."

Applicants respectfully remind the Examiner that a Preliminary Amendment so labeling these drawings was filed on December 22, 2003. Thus, no further action need be taken.

Claims 22-24 stand rejected under 35 U.S.C. § 102(a) as anticipated by Applicants' Admitted Prior Art (hereafter, "**APA**").

Applicants respectfully traverse this rejection.

FIG. 37 of **APA** shows first and second conductive patterns, where the first conductive patterns (on the left) are covered with portions of insulating films 119, 122 and 124, capacitors formed of storage electrode 125, dielectric film 130 and opposing electrode 126. The capacitors are covered with insulating film (BPSG layer) 127. The second conductive patterns are covered with insulating films 119, 122, 124 and 127.

Thus, although the second conductive patterns shown in FIG. 37 are covered with four insulating films, the first conductive patterns cannot be said to be covered by two of those insulating films, because at least three of the films are completely interrupted by the storage electrode 125 of the capacitor. Thus, the elements of claim 22 are not anticipated by **APA** under 35 U.S.C. § 102(a).

Furthermore, claims 22-24 read on the third embodiment shown in FIGS. 39A-46, in which the gate electrode of a memory transistor (right side) is covered with insulating layers 225, 240, 242 and 244, while the gate electrode of a logic transistor (left side) is covered only with the insulating layers 242 and 244.

Accordingly, claim 22 has been amended to recite this distinction.

The second, third and fourth insulating layers have different shapes than the first insulating layer in the memory transistor. The insulating layers of the logic transistor are renamed as fifth and sixth insulating films, formed of the same material as that of the third and fourth insulating films. The fifth insulating film is directly formed on the gate electrode (first conductive pattern).

Thus, the 35 U.S.C. § 102(a) rejection should be withdrawn.

In view of the aforementioned remarks, claims 22-24 and 33-40 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

U.S. Patent Application Serial No. 10/707,525
Response to Office Action dated March 10, 2006

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

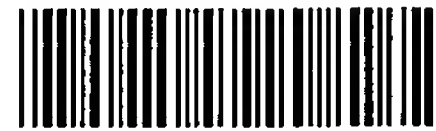
Respectfully submitted,

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Enclosures: Amendment Transmittal
Check in the amount of \$400.00

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